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Team Nexperia

AN11733

Logic data sheet parameters

Rev. 2 — 15 October 2015 Application note

Document information

Info	Content
Keywords	—
Abstract	NXP's standard-logic products data sheets describe the device function, and provide electrical and mechanical specifications including available package types and footprints. These specifications include acronyms, numerical limits, test conditions and data that can be confusing at times for the user to understand. In order to correctly use these devices in a system design and to build robust products, it is critical to fully understand and interpret their specifications and parameters. This application note explains logic device parameters such as absolute maximum, recommended operating conditions, static and dynamic characteristics, timing and noise characteristics, etc., as specified in the data sheets. With the data sheet parameters clearly explained, system designers can use the logic devices within NXP's recommended specifications and ensure maximum system reliability.

Revision history

Rev	Date	Description
v.1	20150923	Draft version.
v. 2	20151015	Release version.

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1. Electrical characteristics

1.1 Currents

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{CC} / I_{DD} (supply current): the current flowing into the V_{CC} / V_{DD} supply terminal.

ΔI_{CC} (additional supply current): the increase in supply current per input pin at the specified input voltage and V_{CC}.

I_{GND} (ground current): the current flowing into the GND terminal.

I_I (input leakage current): the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} (input diode current): the current flowing into a device at a specified input voltage.

I_O (output current): the current flowing into a device at a specified output voltage.

I_{OFF} (power-off leakage current): the current flowing into a device at a specified voltage when V_{CC} = 0 V.

I_{OZ} (OFF-state output current): the current flowing into a 3-state output in the OFF-state at a specified output voltage and V_{CC}.

I_{OH} (HIGH-level output current): the current flowing into an output that is driving HIGH at a specified output voltage and V_{CC}.

I_{OL} (LOW-level output current): the current flowing into an output that is driving LOW at a specified output voltage and V_{CC}.

I_{BHL} (bus hold LOW current): the current flowing into a bus hold input set LOW at a specified input voltage and V_{CC}.

I_{BHH} (bus hold HIGH current): the current flowing into a bus hold input set HIGH at a specified input voltage and V_{CC}.

I_{BHLO} (bus hold LOW overdrive current): the current required to switch a bus hold input from a LOW to HIGH at a specified V_{CC}.

I_{BHHO} (bus hold HIGH overdrive current): the current required to switch a bus hold input from a HIGH to LOW at a specified V_{CC}.

$I_{O(pu/pd)}$ (power-up/power-down output current): the current flowing into an output during power-up or power-down at a specified output voltage and V_{CC}.

1.2 Voltages

All voltages are referenced to GND or V_{SS}, the most negative potential applied to the device.

GND / V_{SS} (supply voltage): for a device with a single negative power supply, the most negative power supply. Used as the reference level for other voltages; typically ground.

V_{CC} / V_{DD} (supply voltage): the most positive potential on the device.

V_{EE} (supply voltage): one of two (GND and V_{EE}) negative power supplies. For a device with dual negative power supply, the most negative power supply.

V_I (input voltage): the range of voltages that can be applied to an input pin.

V_O (output voltage): the range of voltages that can be applied to an output pin.

V_{IH} (HIGH-level input voltage): the range of input voltages that represents a logic HIGH level in the system.

V_{IL} (LOW-level input voltage): the range of input voltages that represents a logic LOW level in the system.

V_{OH} (HIGH-level output voltage): the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} (LOW-level output voltage): the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{T+} (positive-going threshold): the input voltage threshold that represents a logic HIGH level in the system.

V_{T-} (negative-going threshold): the input voltage threshold that represents a logic LOW level in the system.

V_H (hysteresis): the difference between the positive-going and negative-going thresholds.

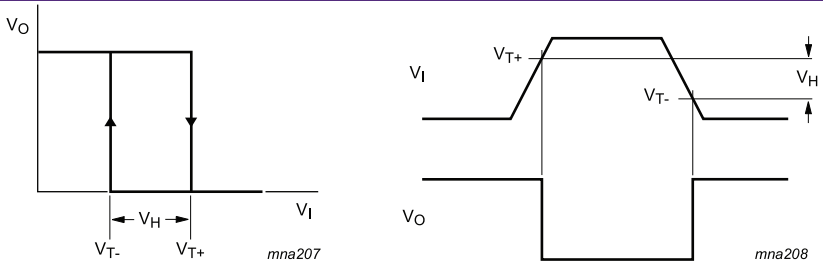

Figure 1. Transfer characteristics showing V_O versus V_I

Built in DC hysteresis in logic devices is useful in systems where inputs have some noise due to electromagnetic induction, or cross talk etc. Each input has immunity against noise depending on the amount of hysteresis voltage present.

2. Typical data sheet view

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	-	5.5	V
T_{amb}	ambient temperature		−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	– 40 °C to +85 °C			– 40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65V_{CC}	-	-	0.65V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7V_{CC}	-	-	0.7V_{CC}	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35V_{CC}	-	0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3V_{CC}	-	0.3V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = −100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1	-	-	V_{CC} – 0.1	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	-	-	0.95	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.9	-	-	1.7	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	-	-	1.9	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.3	-	-	2.0	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.8	-	-	3.4	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	-	0.80	V

Figure 2. Typical data sheet example

3. Analog switches

R_{ON} (ON resistance): the effective ON state resistance of an analog switch, at a specified voltage across the switch, output load and V_{CC}.

$R_{ON(peak)}$ (ON resistance (peak)): the maximum ON state resistance of an analog switch, over the allowed input voltage range.

$R_{ON(rail)}$ (ON resistance (rail)): the ON state resistance of an analog switch, at an input voltage equal to supply voltage or ground.

ΔR_{ON} (ON resistance mismatch between channels): the difference in ON resistance between any two analog switches within a device.

R_{ON}(flat) (ON resistance (flatness)): the difference in ON resistance of an analog switch over the allowed input voltage range.

$C_{S(ON)}$ (ON-state capacitance): the internal capacitance seen at an analog switch terminal when the switch is closed or ON.

$C_{S(OFF)}$ (OFF-state capacitance): the internal capacitance seen at an analog switch terminal when the switch is open or OFF.

V_{ct} (crosstalk voltage): crosstalk between digital inputs and an analog switch terminal, at a specified input signal and load.

Xtalk (crosstalk): crosstalk between different analog switch terminals, at a specified input signal and load.

$f_{(-3dB)}$ (-3 dB frequency response): bandwidth of an analog switch, at a specified input signal and load.

THD (total harmonic distortion): total harmonic distortion of a signal due to an analog switch, at a specified input signal and load.

α_{iso} (isolation (OFF-state)): OFF-state isolation between terminals of a disabled analog switch, at a specified input voltage and load.

Qinj (charge injection): charge injected from a digital control pin to the path of an analog switch, at a specified input voltage and load.

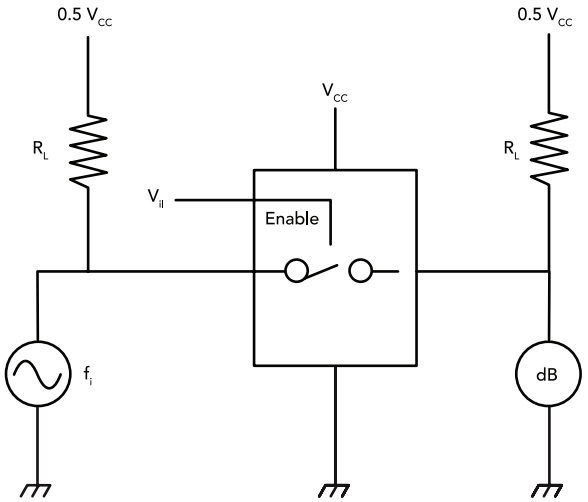

Figure 3. Off Isolation test circuit

Charge Injection: As the switch turns ON or OFF, small amounts of charge can be injected from digital control signal in the path of analog control signals. It can also be seen as enable to output cross talk i.e. changing the state on control pin causes a charge to be coupled on the channel of transistor introducing signal noise.

Total Harmonic Distortion: When a signal passes through a non-ideal, non-linear device, additional content is added at the harmonics of the original frequencies. THD is a measurement of the extent of that distortion. Mathematically, THD can be defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

Lesser THD allows the components in a loudspeaker, amplifier or microphone or other equipment to produce a more accurate reproduction by reducing harmonics added by electronics and audio media. A THD rating < 1% is considered to be in high-fidelity and inaudible to the human ear.

4. AC switching parameters

Δt/ΔV (input transition rise and fall rate): the rate at which the inputs are permitted to change from LOW to HIGH or HIGH to LOW.

t_r (rise time): time taken for a signal to rise, usually measured from 10% to 90% of final level.

t_f (fall Times): time taken for a signal to fall, usually measured from 90% to 10% of final level.

t_{pd} (propagation delay): the time required for a transition of an input to produce a transition on an output, at a specified output load and V_{CC}.

t_{PLH} (LOW to HIGH propagation delay): the time required for a transition of an input to produce a LOW to HIGH transition on an output, at a specified output load and V_{CC}.

t_{PHL} (HIGH to LOW propagation delay): the time required for a transition of an input to produce a HIGH to LOW transition on an output, at a specified output load and V_{CC}.

t_{TLH} (LOW to HIGH output transition time): the time required for an output signal to rise, usually measured from 10% to 90% of the final level.

t_{THL} (HIGH to LOW output transition time): the time required for an output signal to fall, usually measured from 10% to 90% of the final level.

t_W (pulse width): the time between the leading and trailing edges of a pulse, at specified levels and V_{CC}.

t_h (hold time): the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input in order to ensure continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_{su} (set-up time): the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input in order to ensure recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} (HIGH to OFF-state propagation delay): the time required for a transition of an input to produce a HIGH to OFF-state transition on an output, at a specified output load and V_{CC}.

t_{PLZ} (LOW to OFF-state propagation delay): the time required for a transition of an input to produce a LOW to OFF-state transition on an output, at a specified output load and V_{CC}.

t_{PZH} (OFF-state to HIGH propagation delay): the time required for a transition of an input to produce an OFF-state to HIGH transition on an output, at a specified output load and V_{CC}.

t_{PZL} (OFF-state to LOW propagation delay): the time required for a transition of an input to produce an OFF-state to LOW transition on an output, at a specified output load and V_{CC}.

t_{en} (enable time): the time required for a transition of an input to produce an OFF-state to LOW transition or an OFF-state to HIGH transition on an output, at a specified output load and V_{CC}.

t_{dis} (disable time): the time required for a transition of an input to produce a LOW to OFF-state transition or a HIGH to OFF-state on an output, at a specified output load and V_{CC}.

t_{rec} (recovery time): the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input.

$t_{sk(o)}$ (output skew time): the difference in propagation delay of outputs of a single device with all inputs switching simultaneously, under identical load conditions.

f_i (input frequency): the frequency of a signal applied to an input.

f_o (output frequency): the frequency of an output signal.

f_{max} (maximum frequency): the maximum frequency of operation. Outputs should switch between 10% and 90% of V_{CC}.

C_i (input capacitance): the internal capacitance of an input pin.

C_o (power dissipation capacitance): the internal capacitance of an output pin.

C_{pd} (power dissipation capacitance): equivalent capacitance value of a device or channel of a device for calculating dynamic power dissipation.

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